N-Channel Synchronous MOSFETs

FUNCTIONAL DESCRIPTION

The SI4724CY is a high-speed driver designed to operate in high frequency dc-dc switchmode power supplies. It is designed to be used with any single output PWM IC or ASIC to produce a highly efficient synchronous rectifier converter.

Under-voltage protection is provided for the Vdd power supply. The device includes a bootstrap diode, integrated Schottky diode, and fast switching times.

MODEL DESCRIPTION

The driver circuit was decomposed into elemental blocks, and then modeled accordingly as per the data sheet and specific topological IC information provided to AEi Systems by Vishay's engineers.

IsSpice models for the output MOSFETs, bootstrap PNP diode, and the Schottky diode were provided and used in the modeling of the SI4724CY. No efforts were made to improve the models although they were reviewed and comments are shown below.

Using ICAP/4, a SPICE package from AEi Systems, a model of the driver was then created using the modules and a corresponding schematic and netlist was generated.

The model includes the following functionality and features:

- Proper transient response including variations with external components.
- Proper connectivity as per the real-life part
- Output rise and fall times for varying loads
- Under voltage lockout & hysteresis
- Switching times (turn off and propagation delays)
- Schottky behavior
- Bootstrap voltage and diode characteristics
- Logic input voltage thresholds
- Break-before-make reference

Note: The variation of the V_{ref} and logic input voltage levels with V_{DD} are not modeled.

The model operation is described as follows:

- V_{DD} under voltage lockout and threshold is modeled by S2, V10, and R5.
- The V_{BBM}/V_{ref}, Sync, and V_{IN} comparisons are handled by B7, B1, and B_{IN}, respectively. The logic input threshold value used was 2.3V. This value is static but could be made a function of V_{IN}.
- The RC combinations, R2/C1, R8/C2 and R7/C1 account for the majority of the IO propagation delays and the T_{ON}/T_{OFF} delay matching.
- The level shifting and the logic functions are modeled by B4 and B5.
- The output FETs have been modeled to provide the appropriate drive performance along with the proper values of r_{DSon} (values used: G1 n-Channel 0.7 Ω/n-Channel 1.5 Ω, G2 n-Channel 0.5 Ω/n-Channel 1 Ω)

ASSUMPTIONS

- Behavior is based on typical values given in the specification sheet for operation at 27 ºC.
- Some thermal variations are modeled including some FET related parameters and the propagation delay and are represented in the subcircuit.
- The SPICE syntax used is compatible with Intusoft ICAP/4. A PSpice version of the subcircuit is also provided.

IS SPICE 4 NETLIST

```
*================================================
* Vishay SI4724CY
*
* This model was developed for Vishay by:
* AEI Systems, LLC
* 5777 W. Century Blvd. Suite 876
* Los Angeles, California 90045
* Copyright 2003, all rights reserved.
*
* This model is subject to change without notice.
* Users may not directly or indirectly re-sell or
* re-distribute this model.
*
* For more information regarding modeling services,
* model libraries and simulation products, please
* call AEi Systems at (310) 216-1144, or contact
* AEi by email: info@aeng.com. http://www.AENG.com
*
* Revision: 6/3/02, version 1.1
* Revision: 1/28/04, version 1.1
* Updated driver voltages and VTO to reduce IC current draw.
* Note, do not trust spice to have accurate currents.
**********
*SRC=Si4724CY;Si4724CY;Drivers;Power Mosfet;Synchronous
*SYM=Si4724CY
.SUBCKT Si4724CY VDD Vin Sync Gnd Boot D1 S1 D2 S2
*               VDD Vin Sync Gnd Boot D1 S1 D2 S2
* #alias bbm  v(bbm)
* #alias g1  v(g1)
* #alias in  v(vin)
* #alias syncin  v(18)
* #alias in2  v(in2)
* #alias in3  v(in3)
* #alias vout  v(5)
* #alias vswitch  v(s1)
* #alias vboot  v(boot)
* #alias vdduvlo  v(vdduvlo)
* #alias g2  v(g2)
V10 Vdd 0 DC=5
B1 15 gnd V=V(Sync) > 2.3 ? 5 : 0
Q1 Boot Boot Vdd SIDRVABSD
.MODEL SIDRVABSD PNP BF=1.2465499 BR=0.0743382
+ CJC=2.48725E-10 CJE=1.45909E-10 EG=1.32 FC=0.5
+ IKF=10.6793593 IKR=100 IRB=9.494516E-6 IS=5.828556E-18
+ ISC=5.929013E-14 ISE=3.690477E-15 MJC=0.3677641
+ MJE=0.3267463 NC=1.47 NE=1.0479867 NF=0.9018194
+ NR=1.0087761 RB=130.4148594 RBM=0.0957343 RC=80
+ RE=1.0245273 TR=7.68E-7 VAF=1E4 VAR=2E4 VJC=0.6097614
+ VJE=0.803 XTB=3.4 XTI=0.5
B5 8 G1 V=V(VDDUvlo) > 1 ? V(16) > 4 ? 5 : 0
R8 11 8 35
C3 G1 11 30p
X3 D2 G2 S2 SIFETADY { }
R2 14 16 200
C1 16 gnd 100p
B2 In2 gnd V=V(16) > 4 ? 5 : 0
R10 15 18 170
C5 18 gnd 200p
B3 In3 gnd V=V(16) > 2.2 ? 5 : 0
BIN 14 gnd V=V(Vin) > 2.3 ? 5 : 0
S2 25 VDDUvlo Vdd 0 _S2_mod
.MODEL _S2_mod SW VT=3.8 VH=.2 ROFF=10meg
V7 25 0 DC=10
R5 VDDUvlo gnd 1
B7 BBM gnd V=V(S1) > 2.4 ? 5 : 0
D3 S2 D2 SISCHC2
.MODEL SISCHC2 D BV=30.2 CJO=200p EG=0.9 FC=0.50 IS=1.5u
+ N=1 RS=0 VJ=0.6 XTI=0.50
B4 27 G2 V=V(VDDUvlo) > 1 ? V(16) < 2.2 ? V(18) > 1 ? V(BBM) < 1 ? 5 : 0
R6 12 27 10
C2 12 G2 20p
X4 D1 G1 S1 SIFETADY { }
M9 S1 11 G1 G1 SIDRVAFETPh
.MODEL SIDRVAFETPh PMOS Level=1 CBD=530p CBS=636p
+ CGBO=1.07u CGDO=650n CGSO=780n GAMMA=0 IS=1.00p KP=75.0m
+ LAMBDA=2.50m MJ=0.460 PB=0.800 PHI=.75 RD=0.210 RS=0.210
+ VTO=2
M10 Gnd 12 G2 G2 SIDRVAFETPL
.MODEL SIDRVAFETPL PMOS Level=1 CBD=530p CBS=636p
+ CGBO=1.07u CGDO=650n CGSO=780n GAMMA=0 IS=1.00p KP=75.0m
+ LAMBDA=2.50m MJ=0.460 PB=0.800 PHI=.75 RD=0.140 RS=0.140
+ VTO=2
M11 Boot 11 G1 G1 SIDRVAFETNh
.MODEL SIDRVAFETNh NMOS Level=1 CBD=530p CBS=636p
+ CGBO=1.07u CGDO=650n CGSO=780n GAMMA=0 IS=1.00p KP=75.0m
+ LAMBDA=2.50m MJ=0.460 PB=0.800 PHI=.75 RD=98.0m RS=98.0m
+ VTO=2
M12 Vdd 12 G2 G2 SIDRVAFETNL
.MODEL SIDRVAFETNL NMOS Level=1 CBD=530p CBS=636p
+ CGBO=1.07u CGDO=650n CGSO=780n GAMMA=0 IS=1.00p KP=75.0m
+ LAMBDA=2.50m MJ=0.460 PB=0.800 PHI=.75 RD=84.0m RS=84.0m
+ VTO=2
.SUBCKT SIFETADY 4 1 2
M1  3 1 2 2 NMOS W=1358279u L=0.50u
M2  2 1 2 4 PMOS W=1358279u L=0.40u
R1  4 3    11E-3 RTEMP
CGS 1 2    450E-12
DBD 2 4    DBD
  .MODEL  NMOS       NMOS (LEVEL  = 3       TOX    = 5E-8
+ RS     = 4.3E-3        RD     = 0       NSUB   = 1.77E17
+ KP     = 2.1E-5        UO     = 650
+ VMAX   = 0             XJ     = 5E-7    KAPPA  = 7E-2
+ ETA    = 1E-4          TPG    = 1
+ IS     = 0           LD     = 0
+ CGSO   = 0             CGDO   = 0       CGBO   = 0
+ NFS    = 0.8E12        DELTA  = 0.1)
.MODEL  PMOS       PMOS (LEVEL  = 3       TOX    = 5E-8
+NSUB   = 2.1E16        TPG    = -1)
.MODEL DBD D (CJO=210E-12 VJ=0.38 M=0.22
+RS=0.01 FC=0.1 IS=1E-12 TT=2.8E-8 N=1 BV=30.2)
.MODEL RTEMP R (TC1=6.5E-3  TC2=5.5E-6)
.ENDS

.ENDS
******
```

Table 1: IsSpice4 Subcircuit Netlist

MODEL VERIFICATION

The test circuit described in the data sheet as Figure 4 was created using ICAP/4, and shown in figure 2. The model was tested as per the manufacturer's datasheet using component values provided by Vishay.

The results of the simulation performance for various model aspects are shown in the following figures.

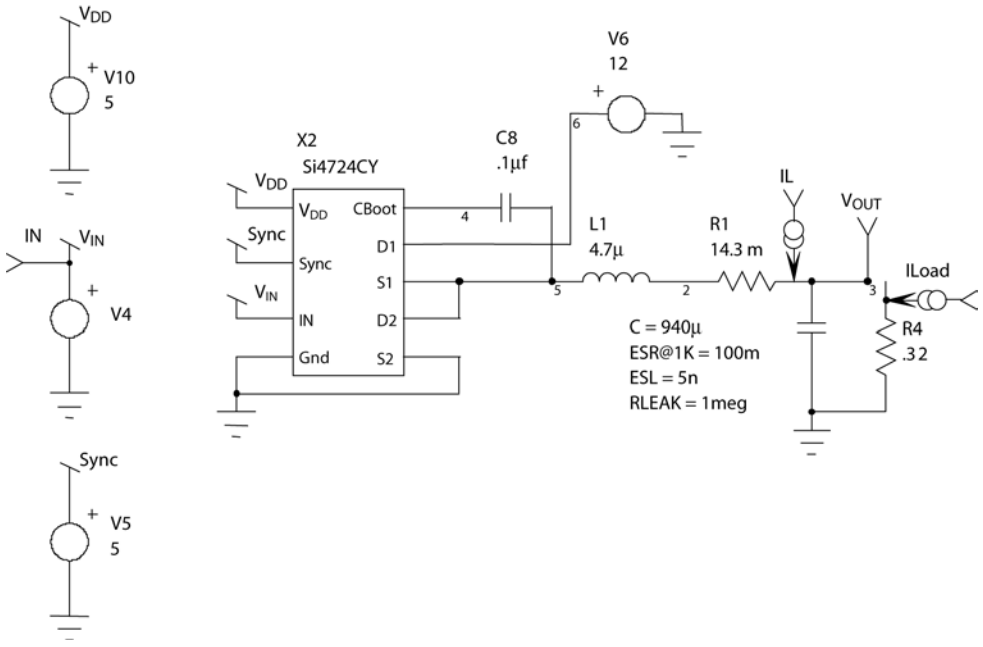

Figure 1: SPICE schematic diagram of the SI4724CY switching test circuit

Note: The configuration in Figure 1 and this schematic were used for propagation delay, delay matching, and rise/fall time tests. Capacitor ESR/ESL and leakage were estimated.

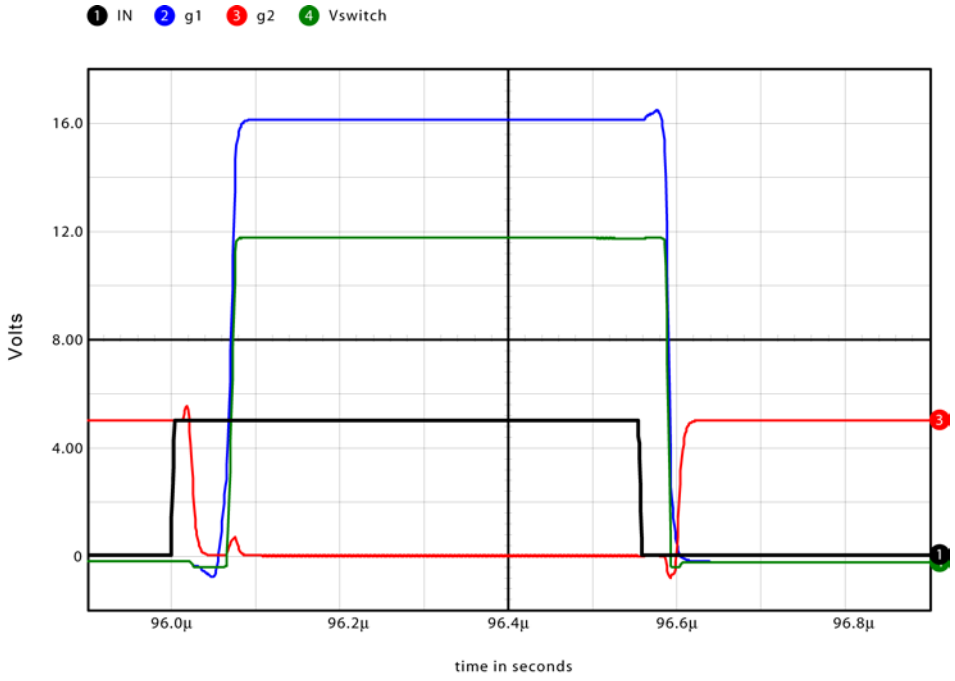

Figure 2: Single input pulse simulation results. Note the dip in Vswitch (green waveform)

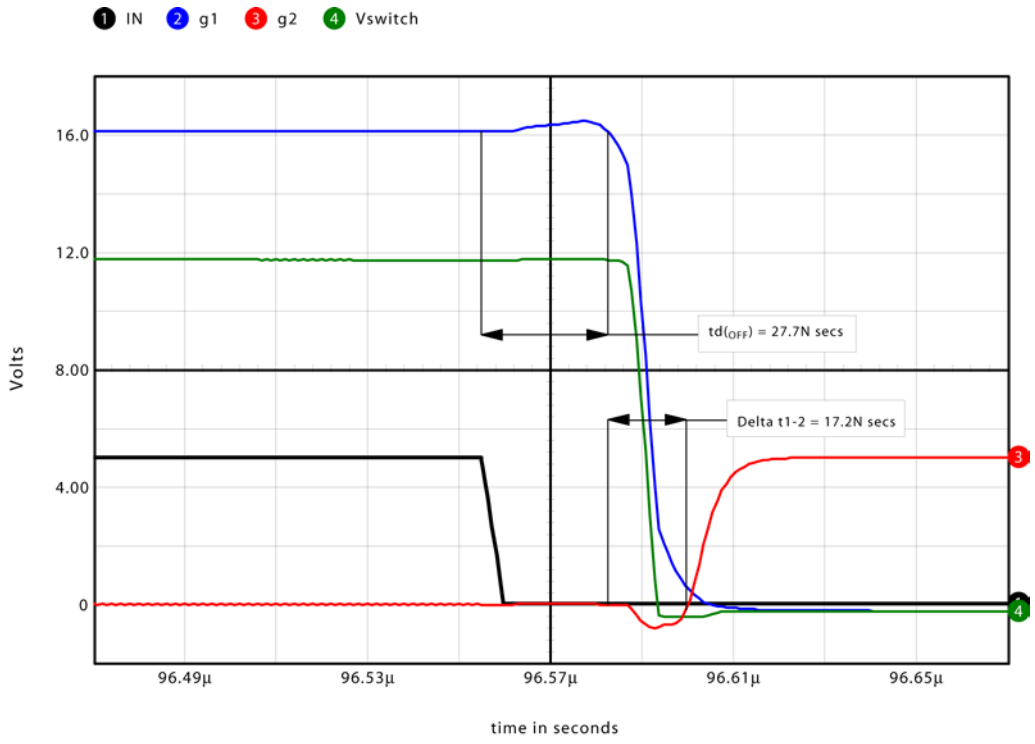

Figure 3: Delta t1-2 Propagation delay simulation results (falling edge of IN)

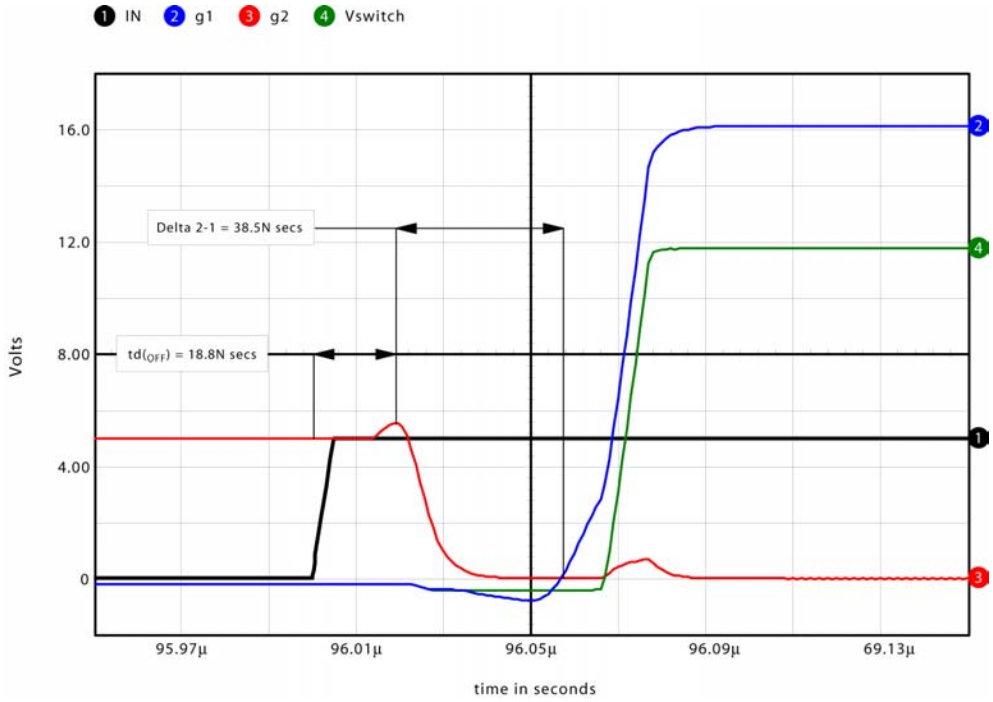

Figure 4: Delta t2-1 Propagation delay simulation results (rising edge of IN)

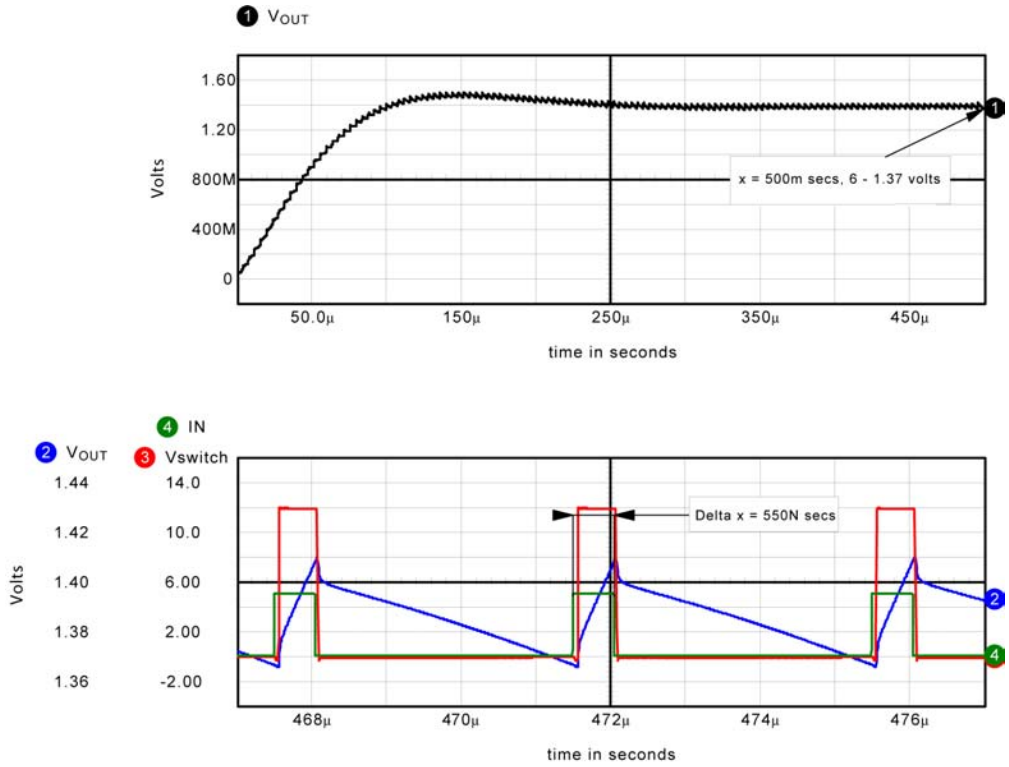

Figure 5: Startup simulation shows V_{OUT} (top graph) and V_{OUT}, Vswitch (S1/D1), and IN (bottom graph)

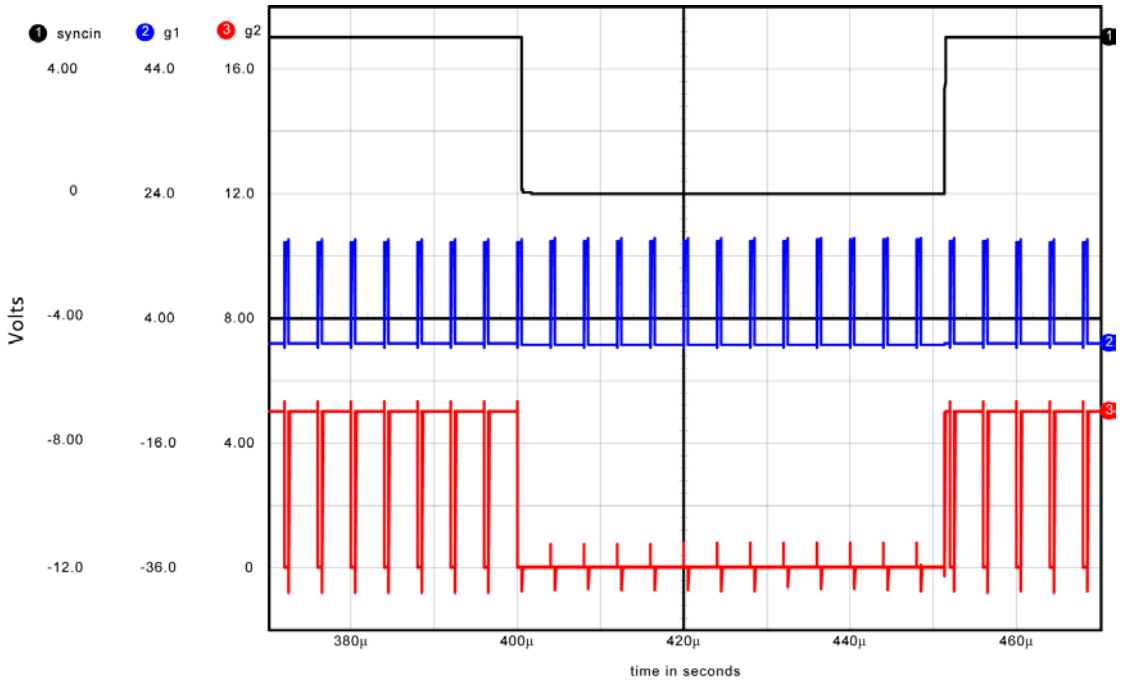

Figure6: Response of the G1 and G2 signals for Sync pulse

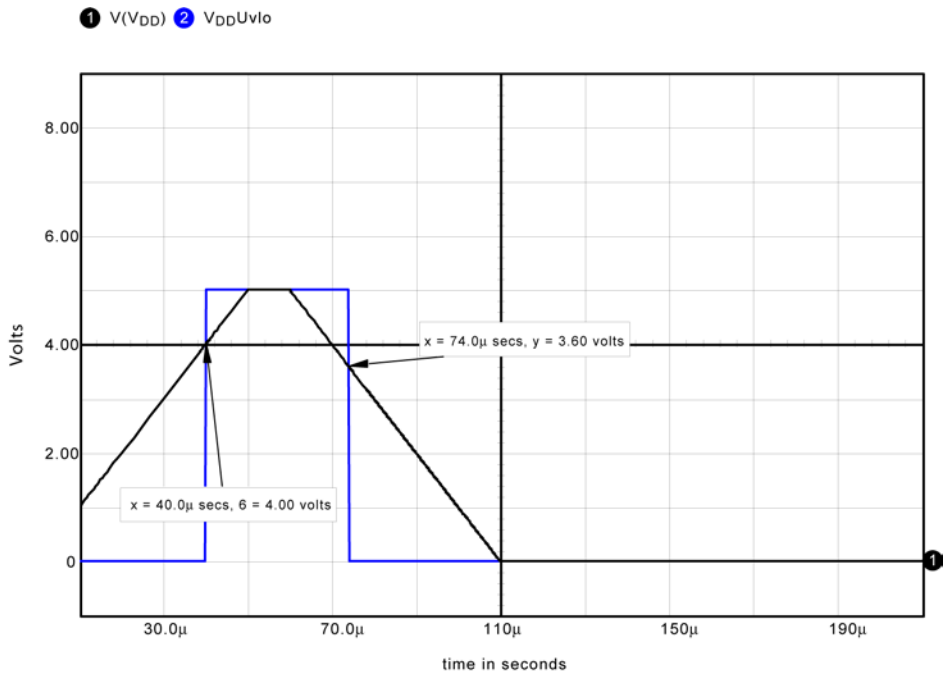

Figure 7: Turn-on/Turn-off and hysteresis for V_{DD}

CONCLUSIONS

The model of the SI4724CY driver correlates very well with the manufacturer's datasheet and meets all of the items listed in the Statement of Work (SOW). This data should be verified against actual hardware for further confirmation.

The output voltage (1.4 V) is somewhat less than the 1.6 V that should be achieved with an input pulse width of 545us (0.545u/4u). The reason for this is unknown.

The variation of the V_{ref} and logic input voltage levels with V_{DD} are not modeled but could be added.

The reader is referred to three references on this topic.

1. "Power Requirements for Power MOSFET Models", I Budihardjo, Peter Lauritzen, A. Mantooth, IEEE Transactions on Power Electronics, Vol 12, No. 1, Jan 1997
2. "An Improved Mosfet Spice Model, Supports the development of Low Dropout Voltage Regulators", Steven M. Sandler, EDATools Café & Internal AEi White Paper, www.edatoolscafe.com/DACafe/TECHNICAL/ Papers/Mosfet_paper.htm
3. "SPICE Model for TMOS", C.E. Cordonnier, Motorola Application Note, AN1043, 1989.

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